## REMARKS

In view of the following discussion, the Applicant submits that none of the claims now pending in the application are non-enabling, anticipated, or obvious under the respective provisions of 35 U.S.C. § 112, §102, and §103. Thus, the Applicant believes that all of these claims are now in allowable form.

It is to be understood that the Applicant, does not acquiesce to the Examiner's characterizations of the art of record or to Applicant's subject matter recited in the pending claims. Further, Applicant is not acquiescing to the Examiner's statements as to the applicability of the prior art of record to the pending claims by filing this Response.

## Objections

**IN THE DRAWINGS:**

The Examiner has objected to the originally filed drawings as they allegedly contain handwritten labeling. In response, Applicant herein submits with this response six (6) pages of formal drawings of FIGs. 1-6 in the subject application. It is respectfully submitted that these newly filed formal drawings are in compliance with all rules and specifically with regard to 37 C.F.R. §1.84. Should the Examiner have additional objections or rejections to these newly filed formal drawings, Applicant requests identification of same in a next Office Action.

## Rejection Of Claims Under 35 U.S.C. §103(a)

The Examiner has rejected claims 1-5, 10-12 and 15-17 under 35 U.S.C. §103 as being obvious and unpatentable over US Patent No. 5,978,359, issued

November 2, 1999 to Caldara, et. al. (hereinafter Caldara) in view of US Patent No. 6,172,963 issued January 9, 2001 to Larsson et. al. (hereinafter Larsson). Specifically, the Examiner has indicated regarding claims 1, 10 and 11 that Caldara discloses a switching architecture that includes a first set of port processors and a second set of port processors. Said sets of port processors can be construed as representing the first and second stages of the subject invention respectively. Caldara also discloses a feedback message (30) that provides an indication of buffer status at the output port. This message is sent in response to a request message (36) which is interpreted to represent the data packet of the present invention (column 5, lines 53-61). The Examiner continues to offer that it is obvious that some component such as a statistic block as in the present invention must count the number of cells in the output buffers and compare them to a threshold level in order to obtain the desired results.

Caldara does not expressly disclose granting credit and an integrator block located in the port processor of the first stage; however, the Examiner offers that Larsson allegedly discloses a credit-based flow control system for a switch with input and output buffers. Larsson allegedly takes into account the degree of fullness of the output buffers when determining how many cells can be sent from each input port. Additionally, with Larsson allegedly showing intelligence in the switch, it can be determined which output ports are able to receive cells, how many cells and from which memory locations. The Examiner offers that this description meets the limitation of an integrator block as in the present application. Specifically, the limitation of neighboring integrator blocks is also met by the fact that each input port has multiple FIFO memories one for each output port. The Examiner continues that at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use the architecture and feedback message of Caldara in combination with the credit-based flow control system of Larsson to provide a switch that selectively sends data from a first stage of input ports to a second stage of output ports in accordance with the fullness or availability of each output buffer. The Examiner

offers additional rejections to dependent claims 2, 3, 4, 5, 12, 15, 16 and 17 based on these combined teachings. The rejection is respectfully traversed.

The test under 35 U.S.C. § 103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Thus, it is impermissible to focus either on the "gist" or "core" of the invention, Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 USPQ 416, 420 (Fed. Cir. 1986) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6 USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added).

The references must be taken in their entireties, including those portions which argue against obviousness. Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 U.S.P.Q. 416, 420 Fed. Cir. 1986). It is impermissible within the framework of the 35 U.S.C. § 103 to pick and choose from a reference only so much of it as will support a conclusion of obviousness to the exclusion of other parts necessary to a full appreciation of what the reference fairly suggests to one skilled in the art. Id. at 419.

**Details of 103 Argument**

Specifically, the Examiner is attempting to combine the teachings of Caldara and Larsson to suggest the subject invention. However, upon closer inspection of these references, deficiencies are seen in each of these references that, upon combination, fail to properly suggest applicant's invention. As indicated by the Examiner, Caldara discloses a feedback message (30) that provides an indication of buffer status at the output port. This message is sent in response to a request message (36) which the Examiner interprets as representing the data packet of the present invention (per column 5 lines 53 to 61

of Caldara). Such interpretation is clearly inaccurate and incorrect upon inspection of the cited portion of Caldara. Such section also indicates that "prior to transmitting a cell from an input port (20) to an output port (22), the request message including the allocated/dynamic tag is sent from the input port to the output port to determine whether sufficient buffers (28) are available in the output port." Accordingly, the reference clearly discloses that there is a difference between data that is sent to and from the output ports (transmission of the cell) and the request message that the Examiner has equated with the data packet. Claim 1 on the subject invention clearly states that the statistics block transmits a token bit in response to the statistics block receiving a data packet. It is respectfully submitted that the request message of Caldara is not the same as the data packet of the subject invention (as information, or data) in Caldara have been identified as cells. Accordingly, data is not transmitted until the request and feedback process has been completed in Caldara.

Moreover, the Examiner has offered that Larsson discloses a process of "giving credit" as per column 3 lines 21 through 30 of the reference. Additionally, the Examiner offers that an intelligent switch disclosed in Larsson can read the degree of fullness of the output buffers and calculate how many cells (data packets) can be sent per column 5 lines 12 to 23 of Larsson. However, the passage of Larsson associated with "giving credit" is far too general to read on or suggest anything specifically claimed. Moreover, the Examiner's offering of intelligence in the switch and the disclosure of multiple FIFO memories meeting the limitation of integrator blocks as recited in independent Claim 1 is also considered far too general to adequately suggest invention. That is, while such multiple FIFO memories may be disclosed, there is no specific description of the organization of such memories in a manner that can be equated with the construction of the statistics and integrator blocks of the first stage and second stage port processors as recited in Claim 1. Applicant offers that such a general description as found in Larsson would require undue experimentation and further development to even attempt to arrive at the circuit configuration of the subject

invention. Accordingly, a combination of Caldara and Larsson results in a system that needs to send a request message and a feedback message prior to sending data through a series of switches that allegedly have some level of intelligence but not necessarily the architecture of statistics and integrator blocks as currently claimed. The Examiner's suggestions are far too reaching to arrive at a conclusion of obviousness with regard to the apparatus of Claim 1.

Similar arguments and conclusions are drawn with regard to the independent method Claim 10. Specifically, the method recites the step of notifying a plurality of first stage port processors in response to receiving a data packet from one of the plurality of first stage port processors and not in response to a request message (which does not include data) followed by a corresponding feedback message in order to practice the subject method. While Larsson attempts to disclose some form of "giving credit" in a data transmission system, it focuses on the aspects of "over-allocation" that allows the input ports to always request to send more cells than the respective output ports can process without placing any cell in its output buffer (column 4 lines 56 through 65). This type of system is not as sophisticated as the subject invention; hence, would not suggest to one skilled in the art to control and manage information traffic flow in the manner claimed. Accordingly, it is respectfully submitted that the combination of Caldara and Larsson fail to suggest the invention recited in independent method Claim 10.

As such, the Applicant submits that claims 1 and 10 are not obvious and fully satisfy the requirements under 35 U.S.C. § 103 and are patentable thereunder. Furthermore, claims 2-9, 11, 12 and 15-17 depend, either directly or indirectly, from independent claims 1 and 10 and recite additional features thereof. As such, and for at least the same reasons discussed above, the Applicant submits that these dependent claims also fully satisfy the requirements under 35 U.S.C. § 103 and are patentable thereunder. Therefore, the Applicant respectfully request that the rejection be withdrawn.

## Conclusion

Thus, the Applicant submits that claims 1-18 are in condition for allowance. Furthermore, the specification has been amended as requested by the Examiner. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Eamon J. Wall at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

August 15, 2003

Respectfully submitted,

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CERTIFICATE OF MAILING under 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited on August 15, 2003 with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Commissioner for Patents, Mail Stop NON-FEE AMENDMENT, P.O. Box 1450 Alexandria, VA 22313-1450.

Janet Kondrk
Signature

August 15, 2003
Date of signature

Janet Kondrk
Type or print name of person signing Certification